

0 0 0 0 0 0 0 0 0 0 0 0

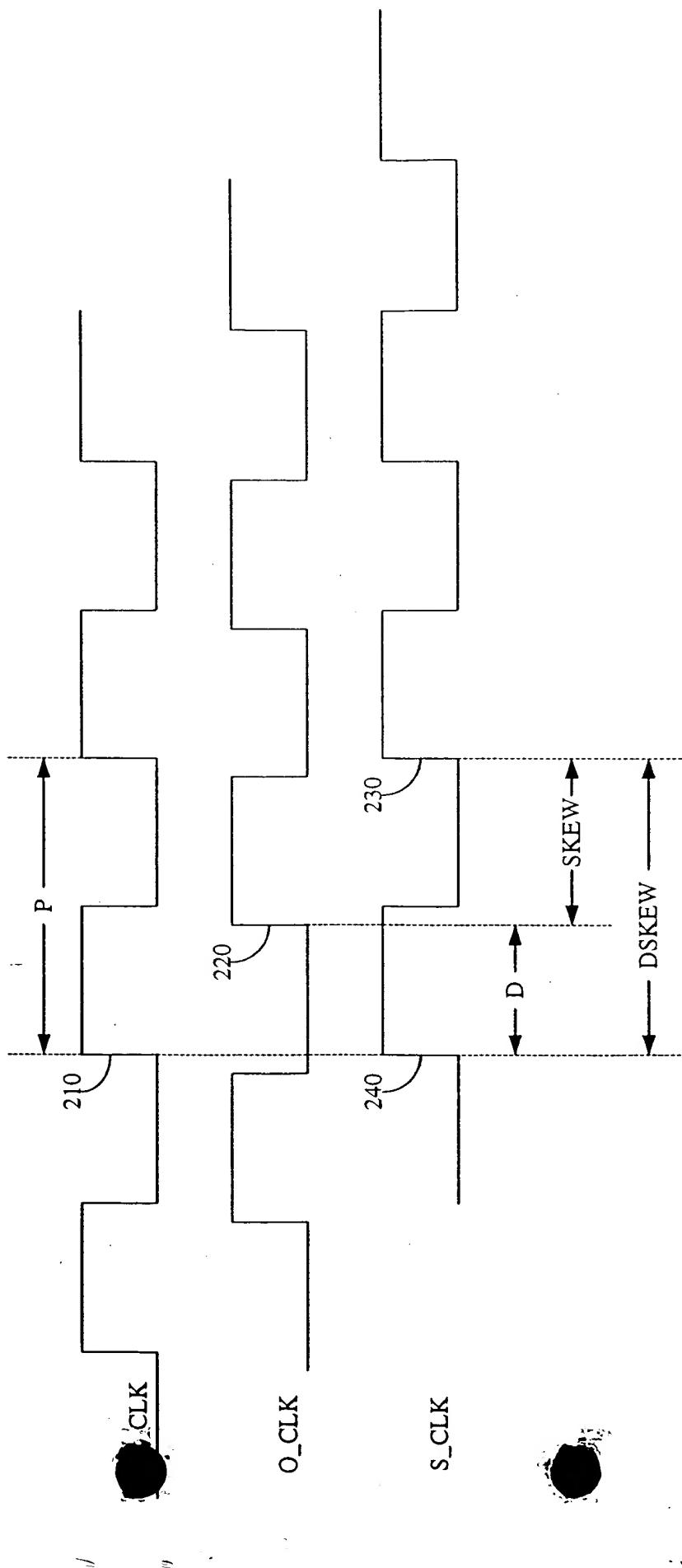


FIGURE 2B

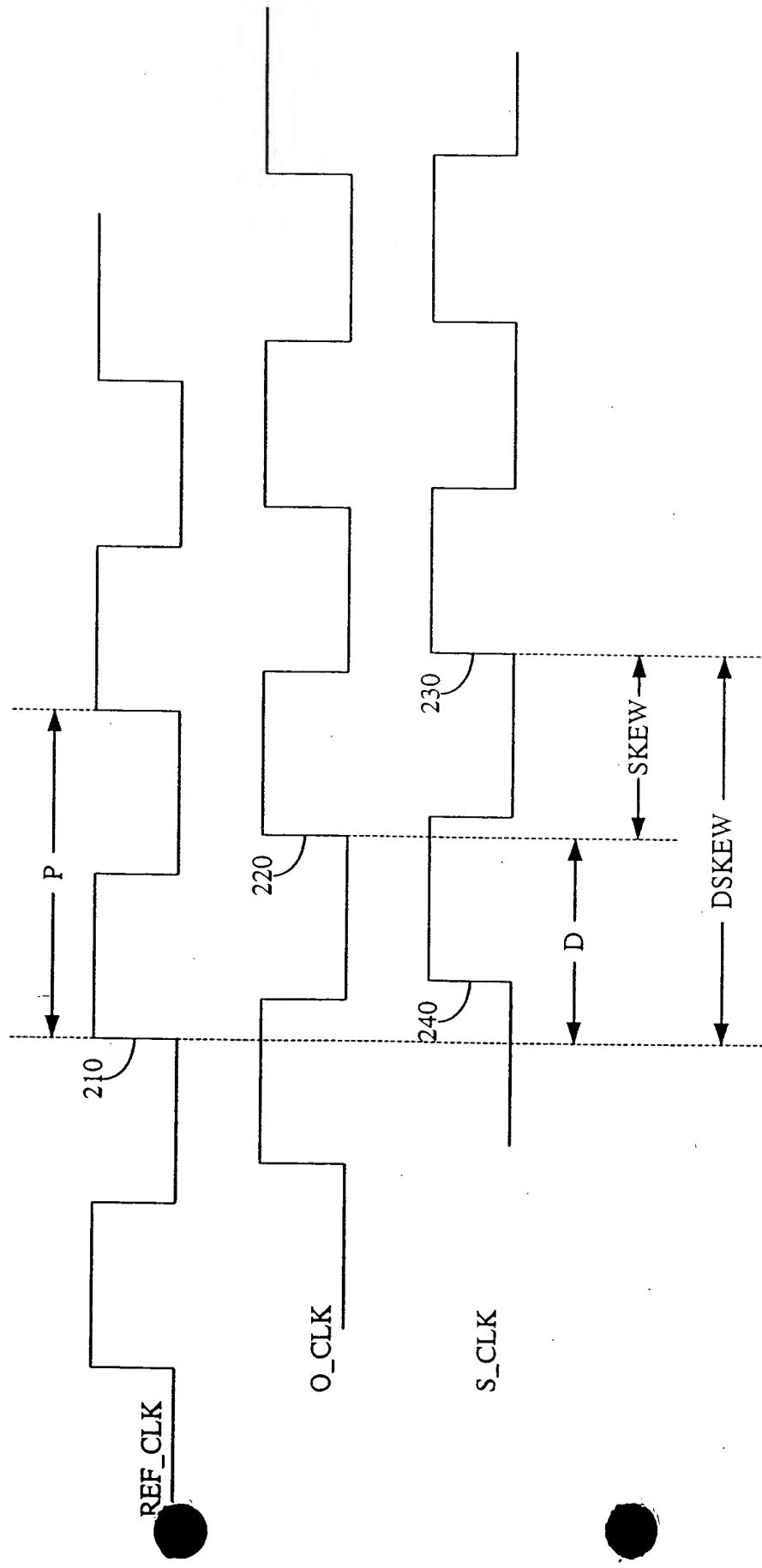


FIGURE 2C

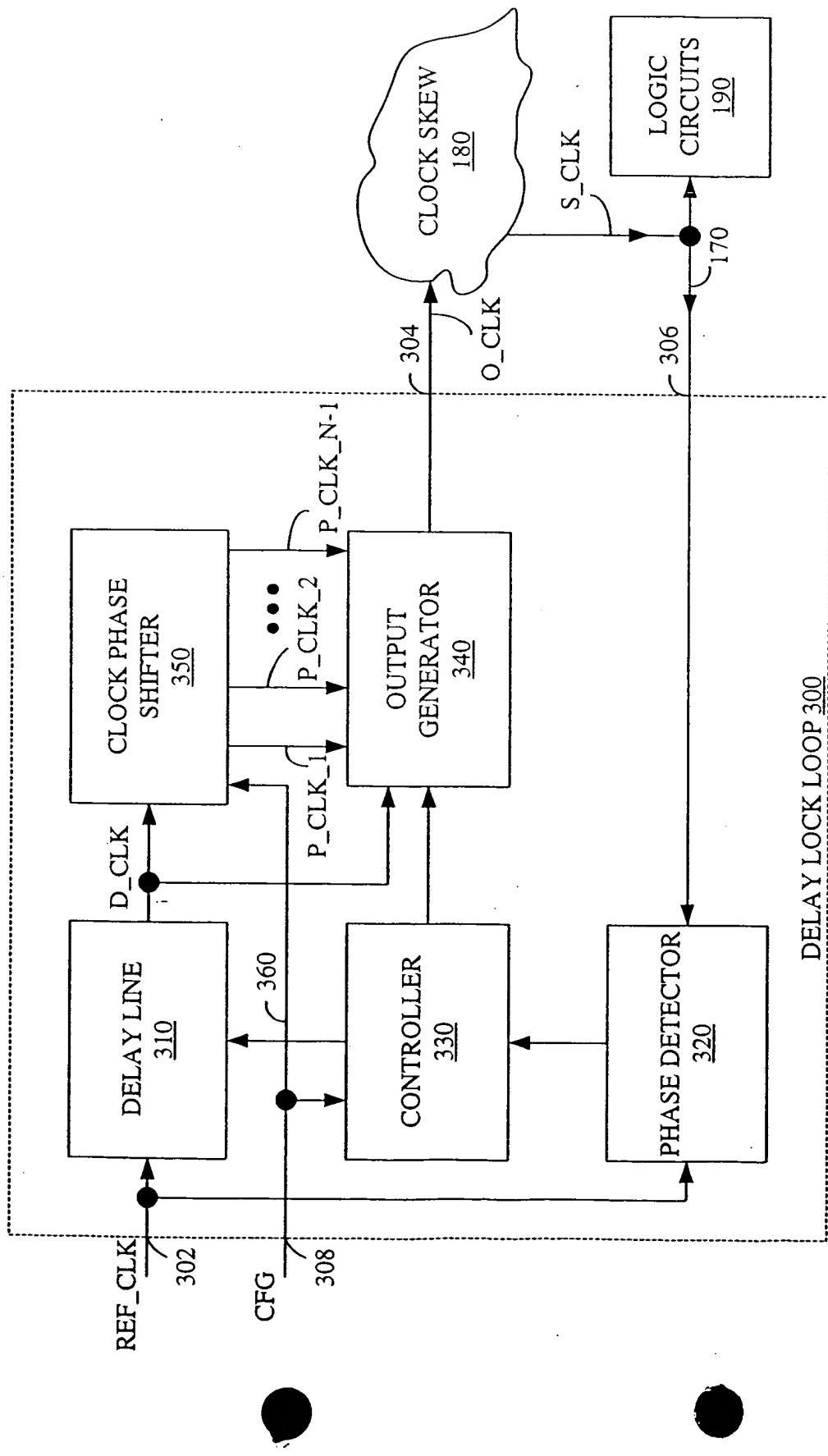


FIGURE 3

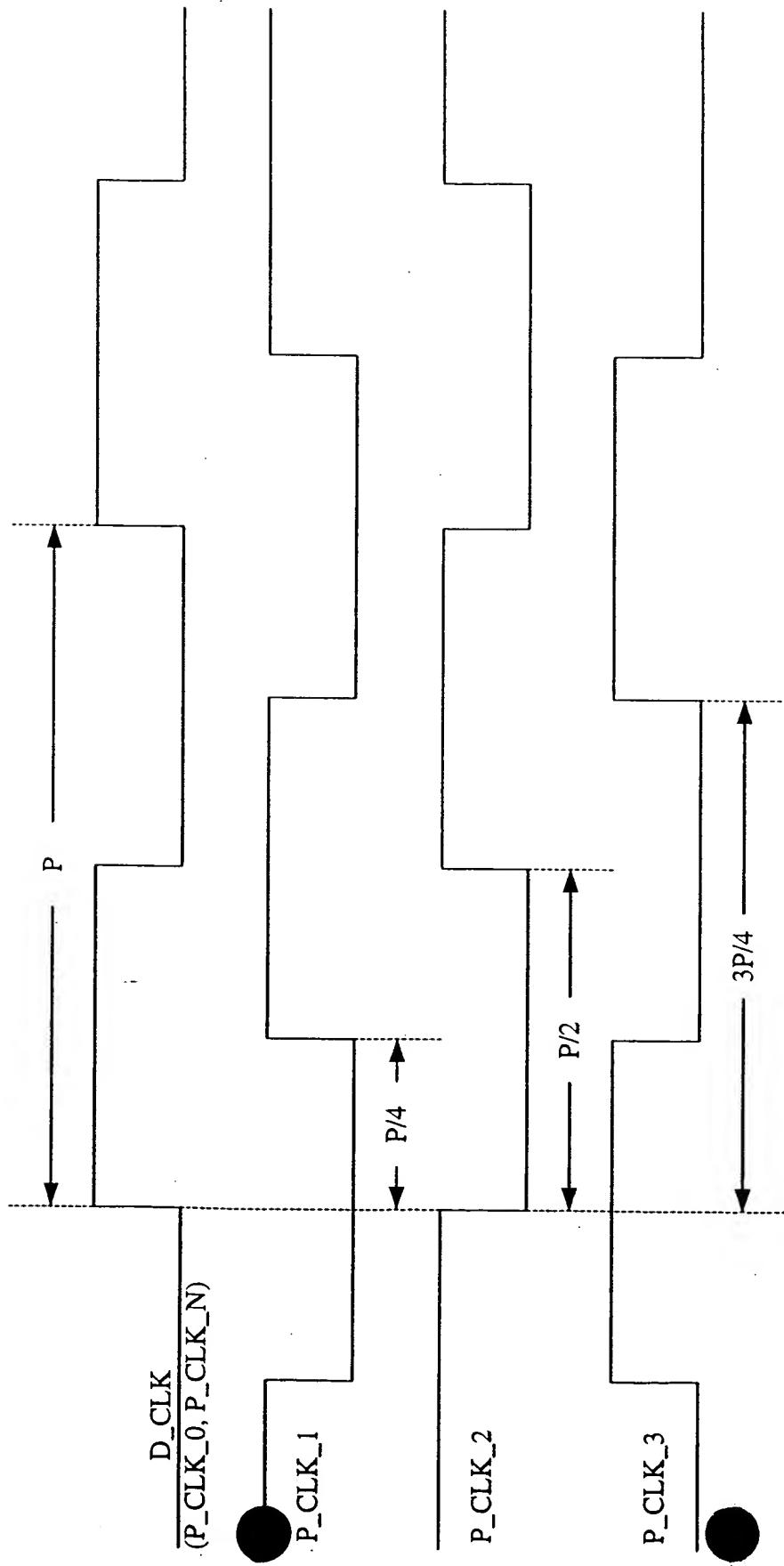


FIGURE 4

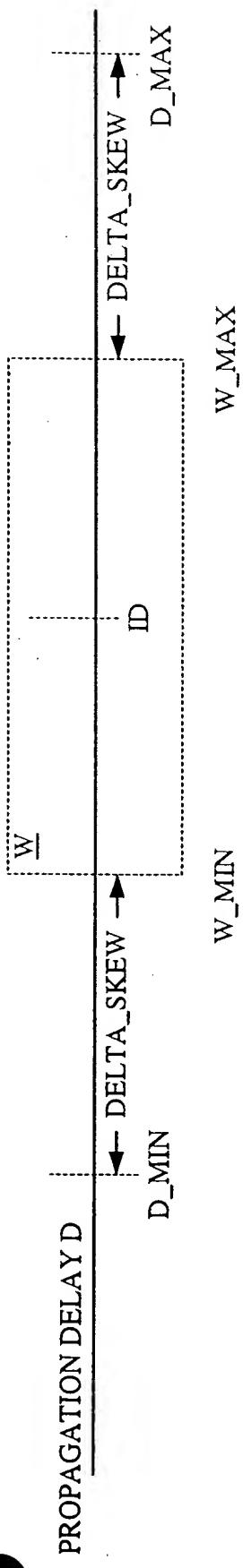


FIGURE 5

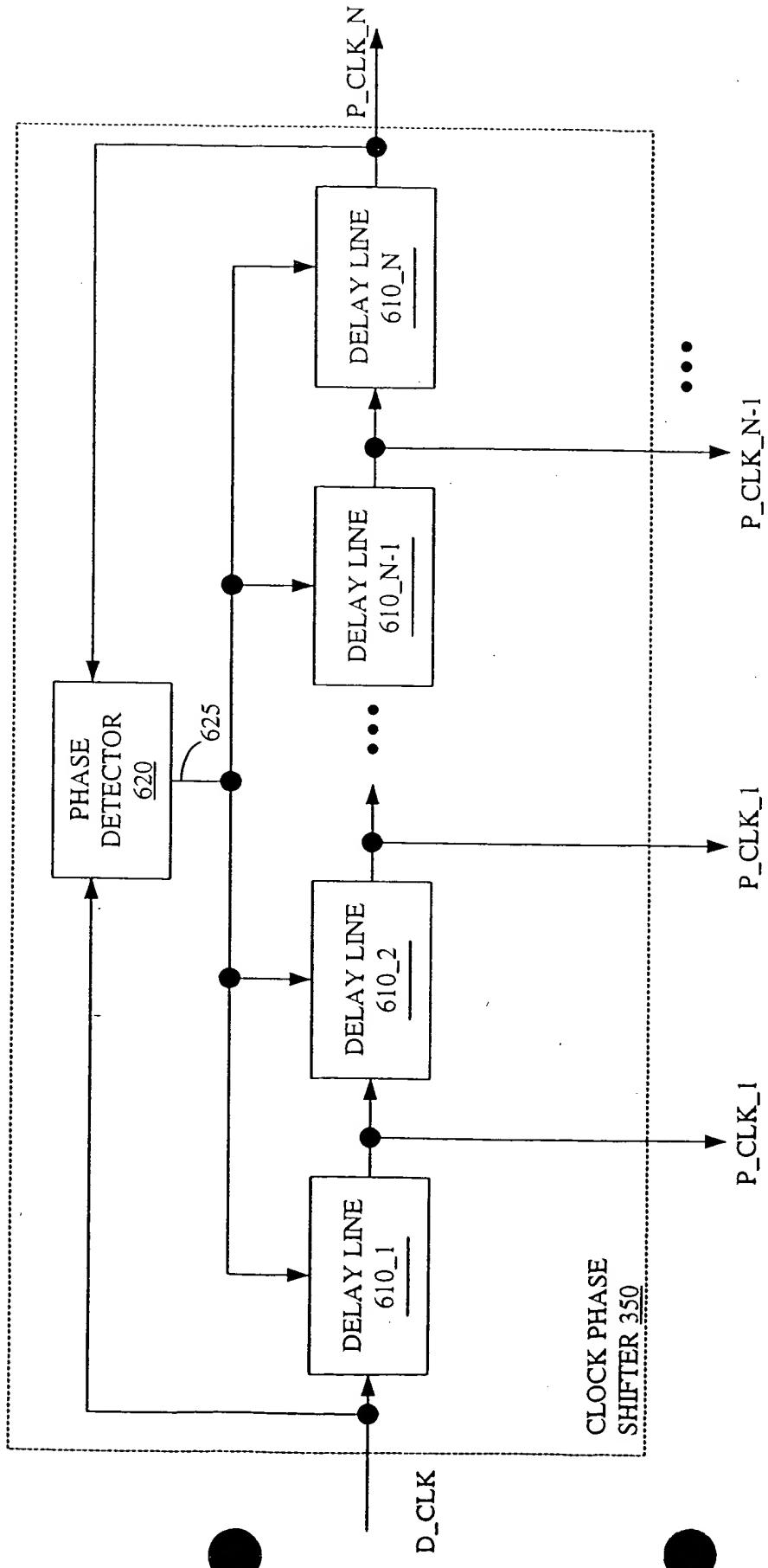


FIGURE 6

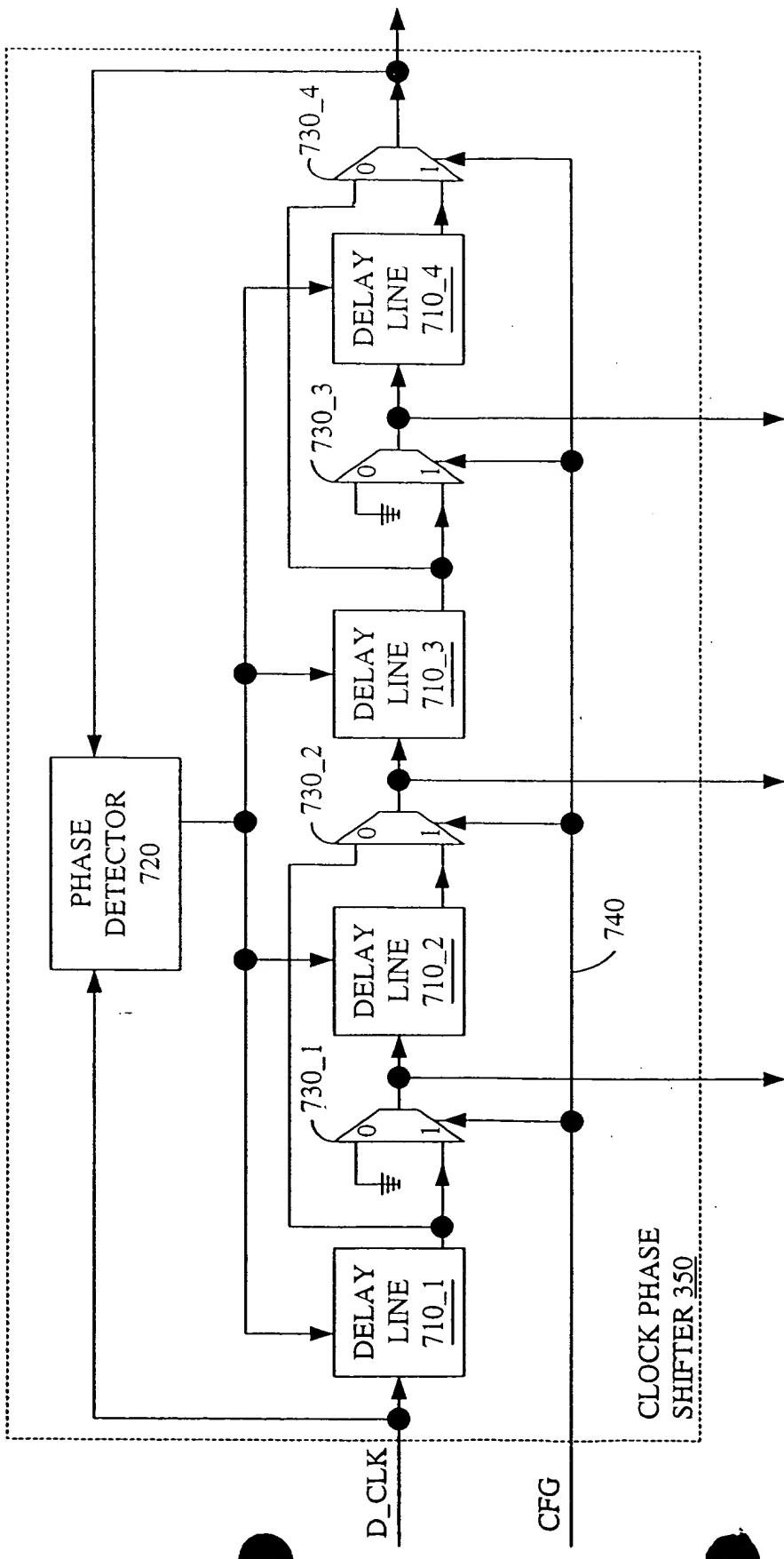


FIGURE 7

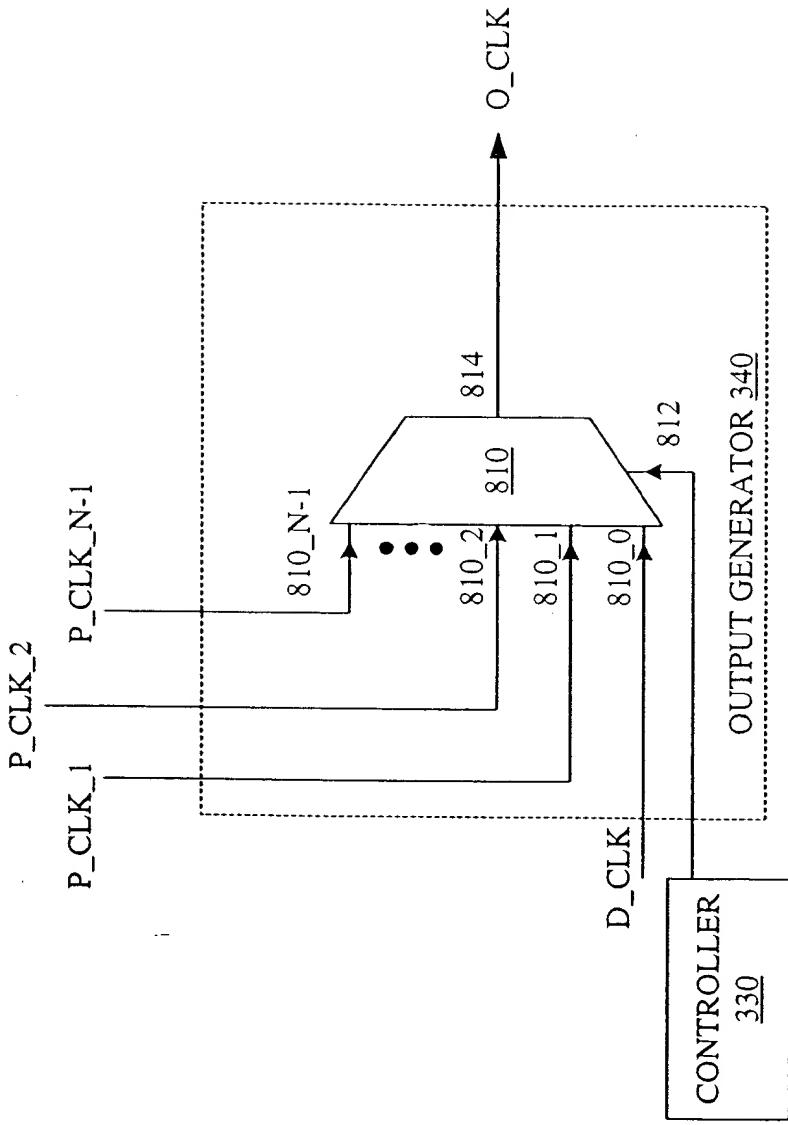
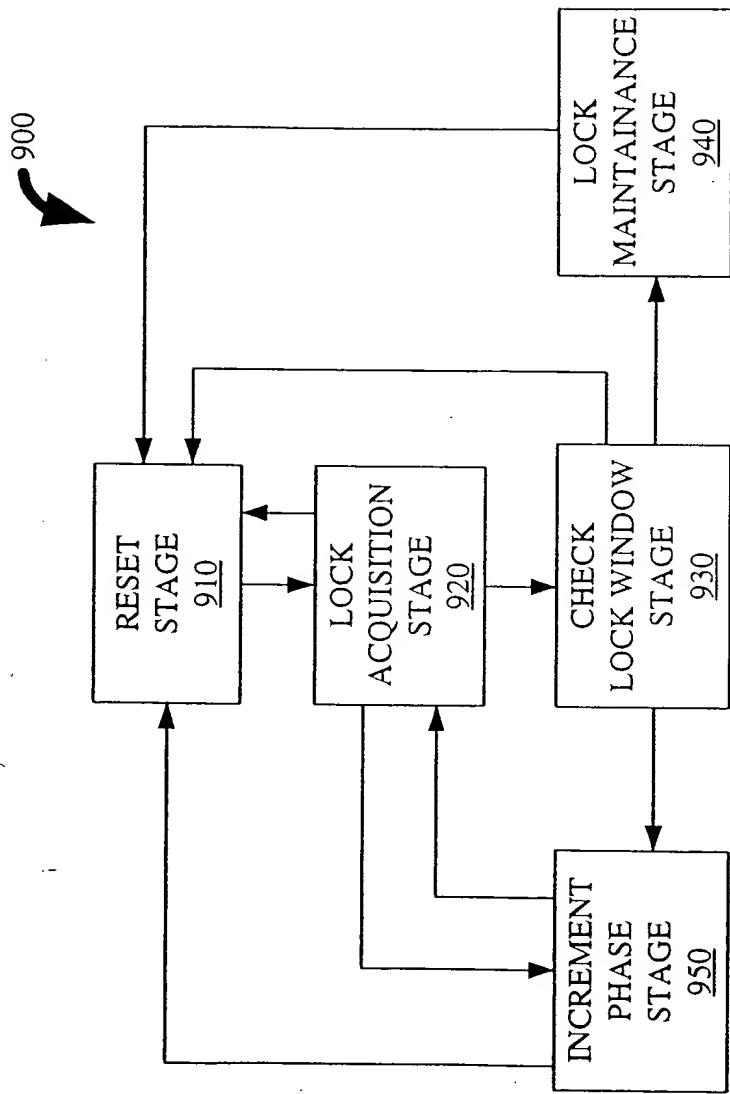


FIGURE 8

FIGURE 9



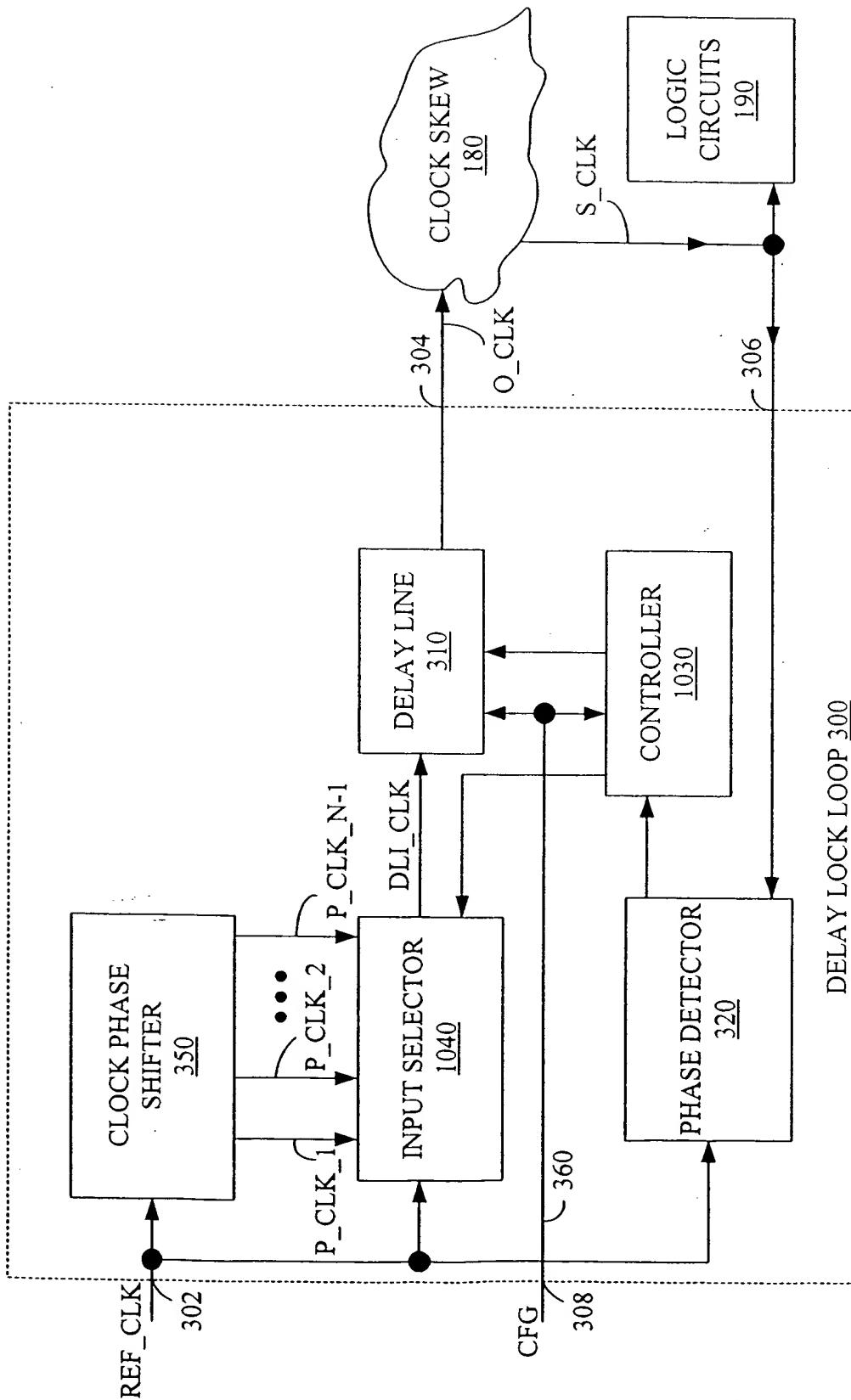


FIGURE 10

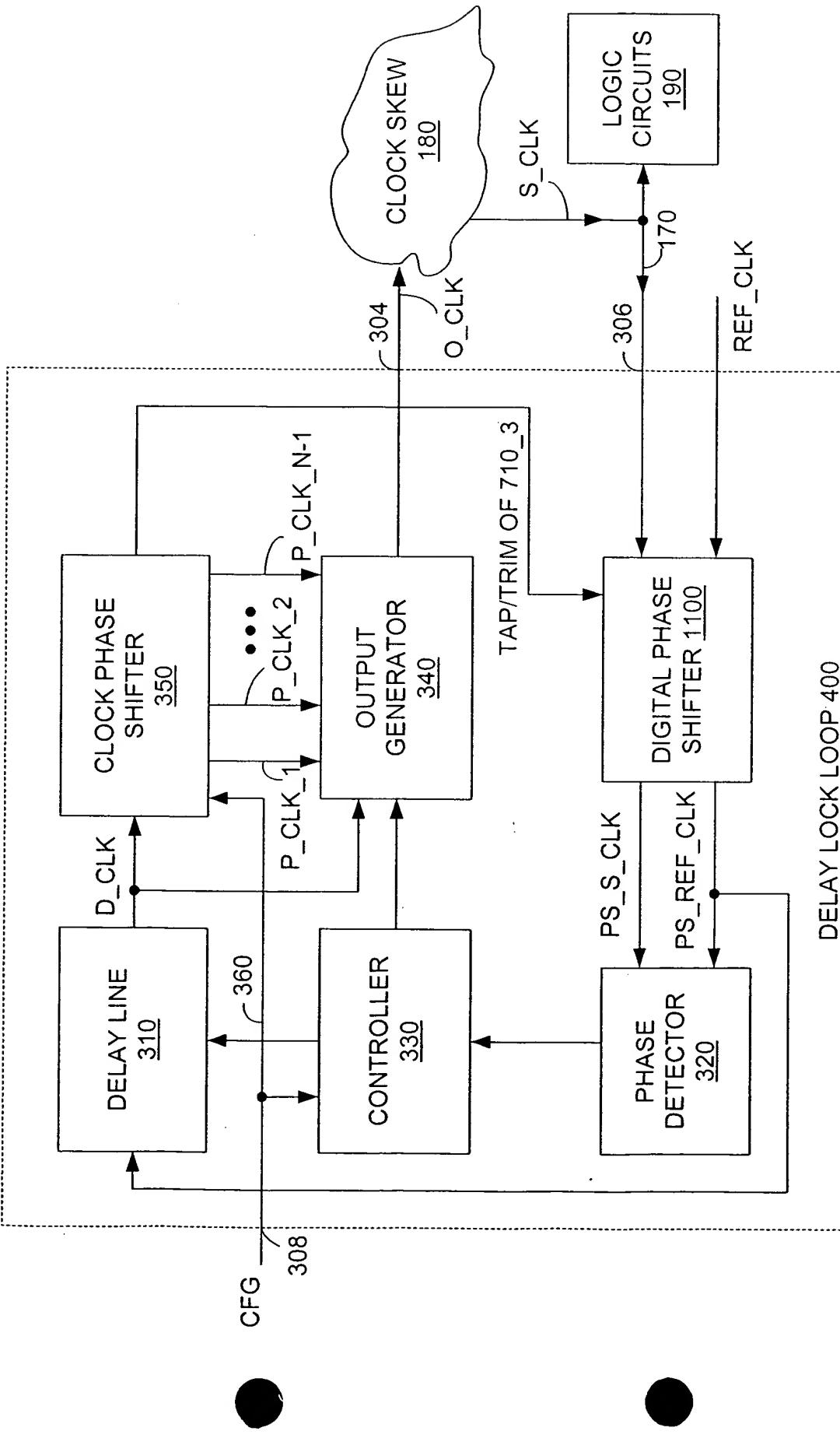


FIGURE 11

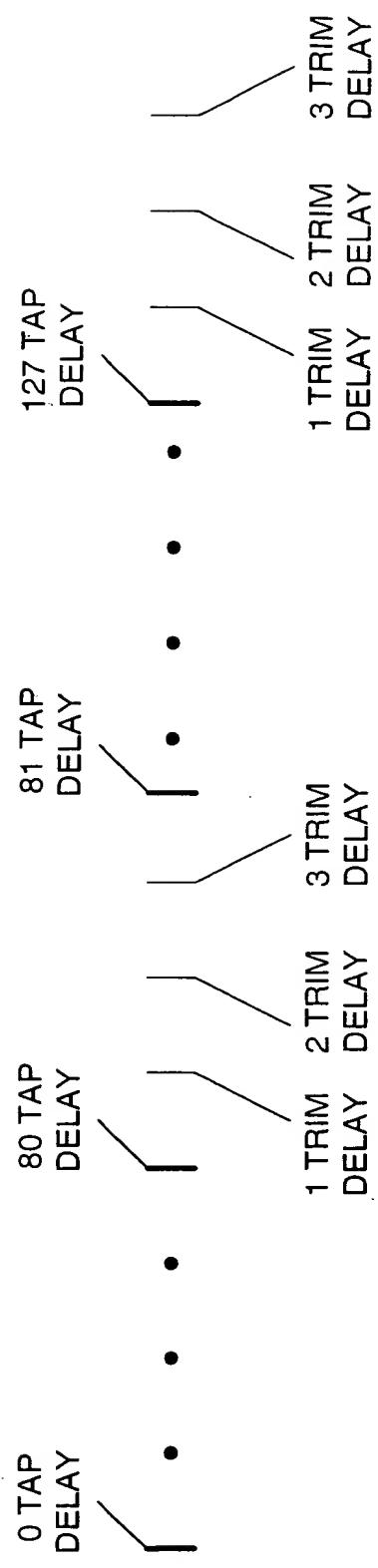


FIG. 12

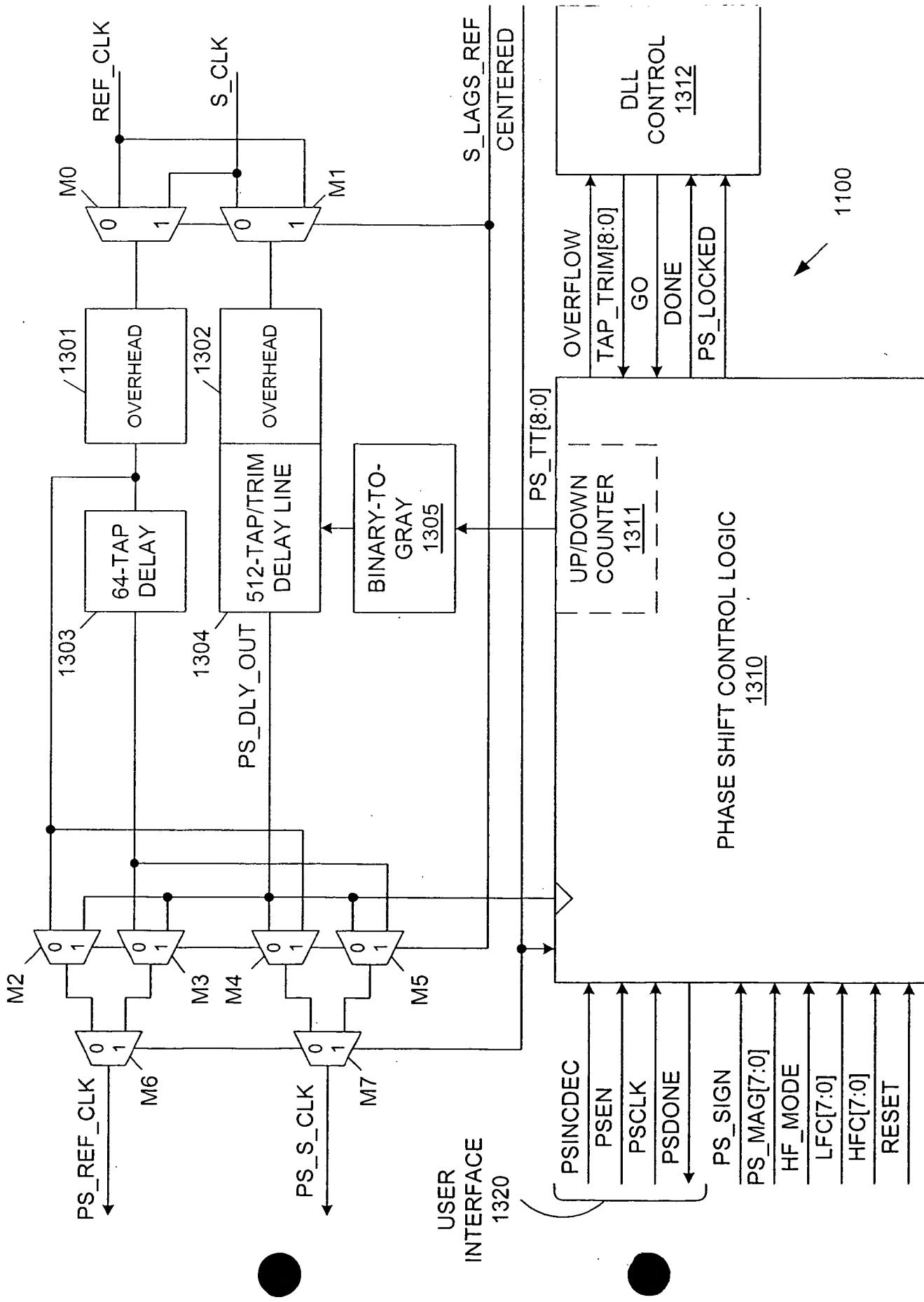


FIG. 13

S_LAGS_REF = 0
CENTERED = 0

FIRST FIXED
MODE

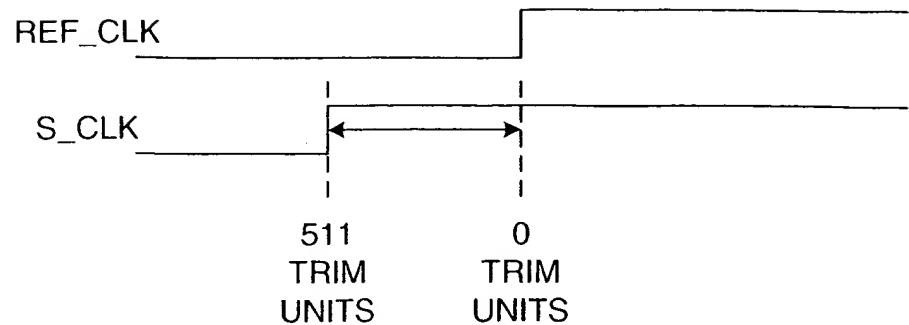


FIG. 14A

S_LAGS_REF = 1
CENTERED = 0

SECOND FIXED
MODE

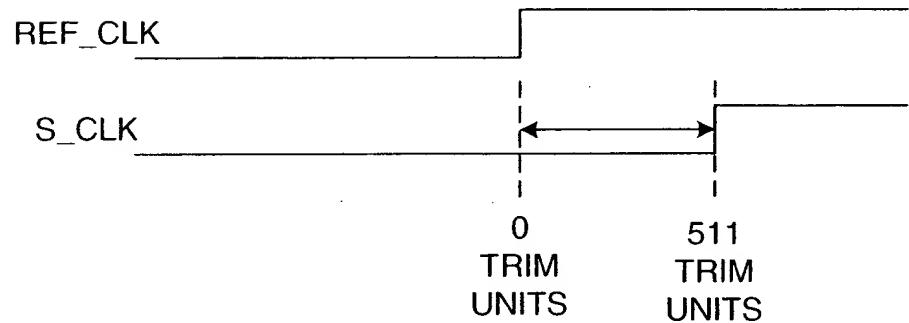


FIG. 14B

S_LAGS_REF =
0 or 1
CENTERED = 1

FIRST AND SECOND
VARIABLE MODES

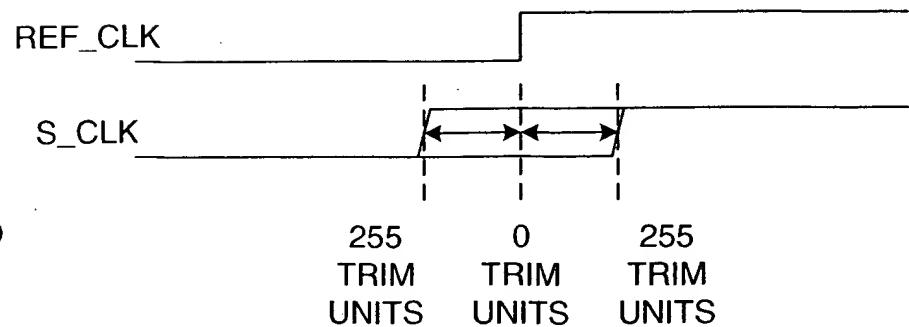


FIG. 14C

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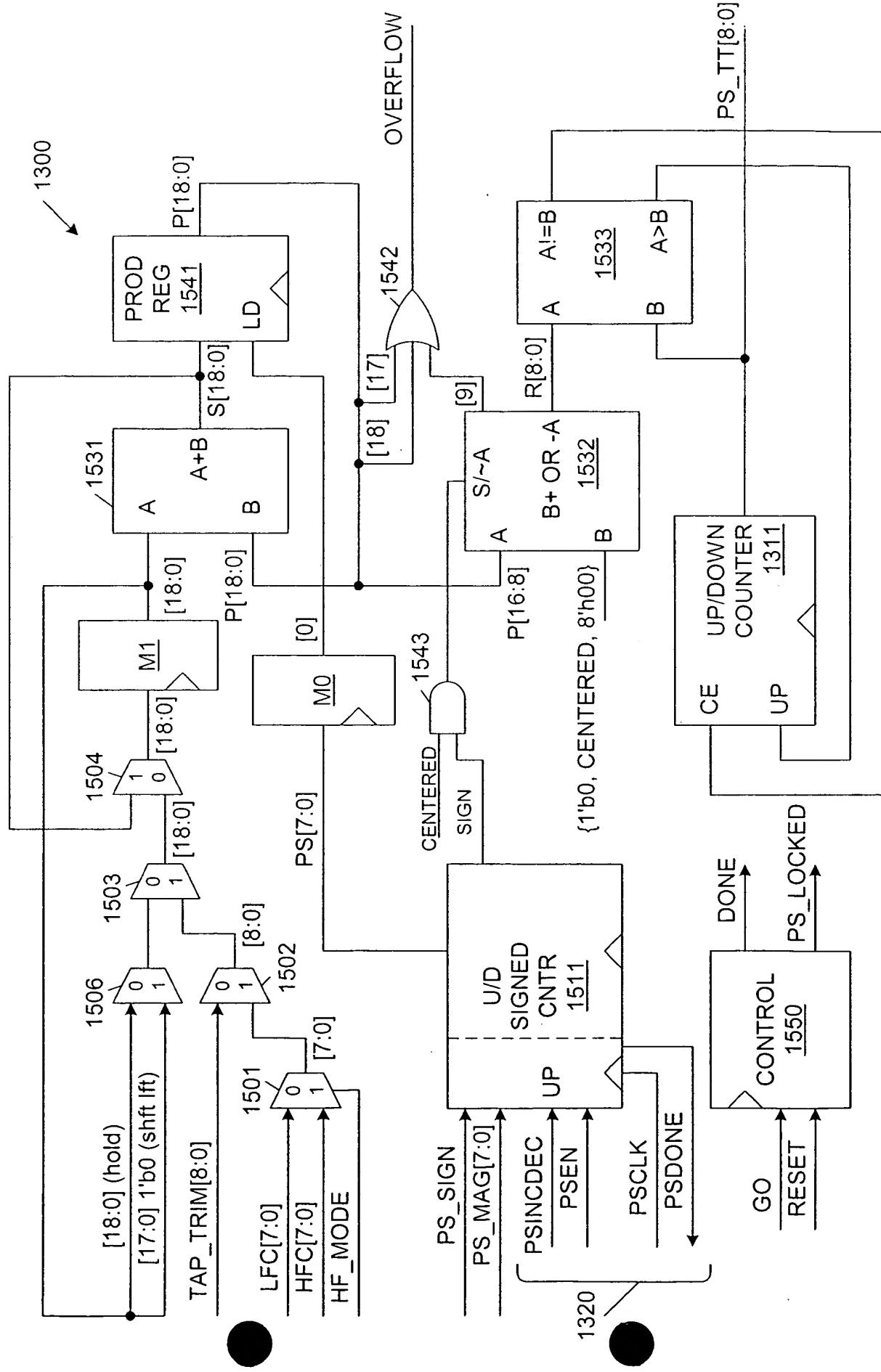


FIG. 15

CLK = PS_DLW_OUT

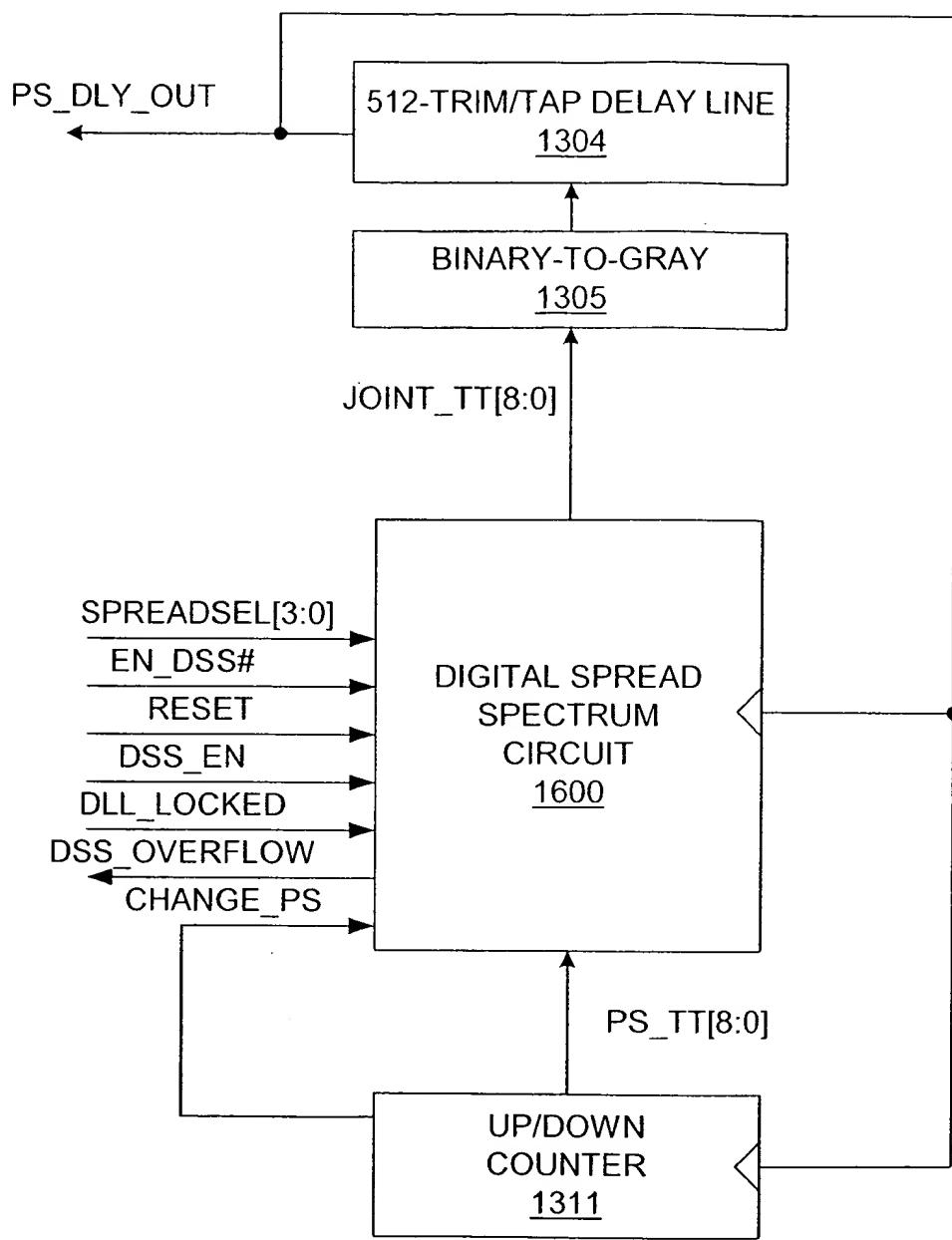


FIG. 16

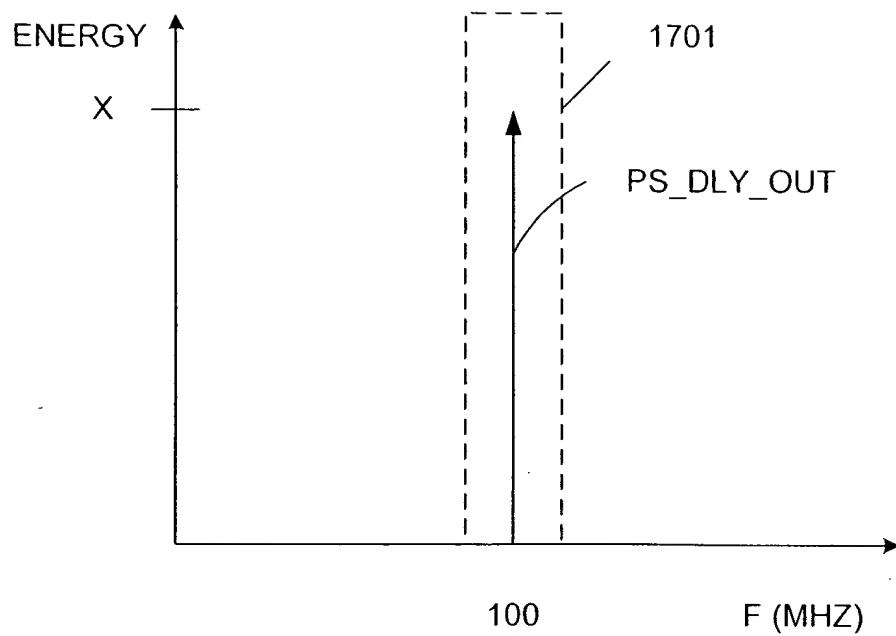


FIG. 17A

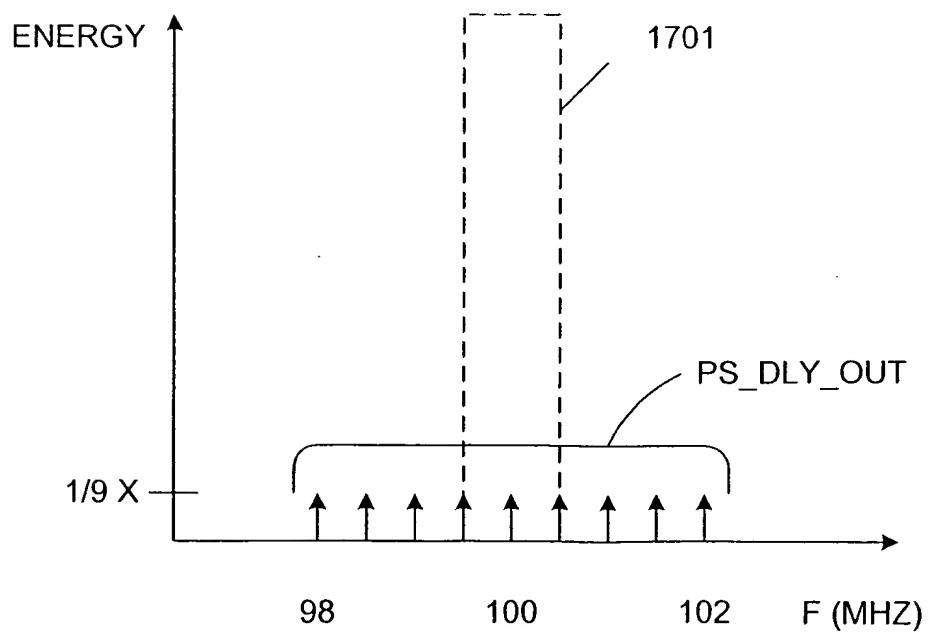


FIG. 17B

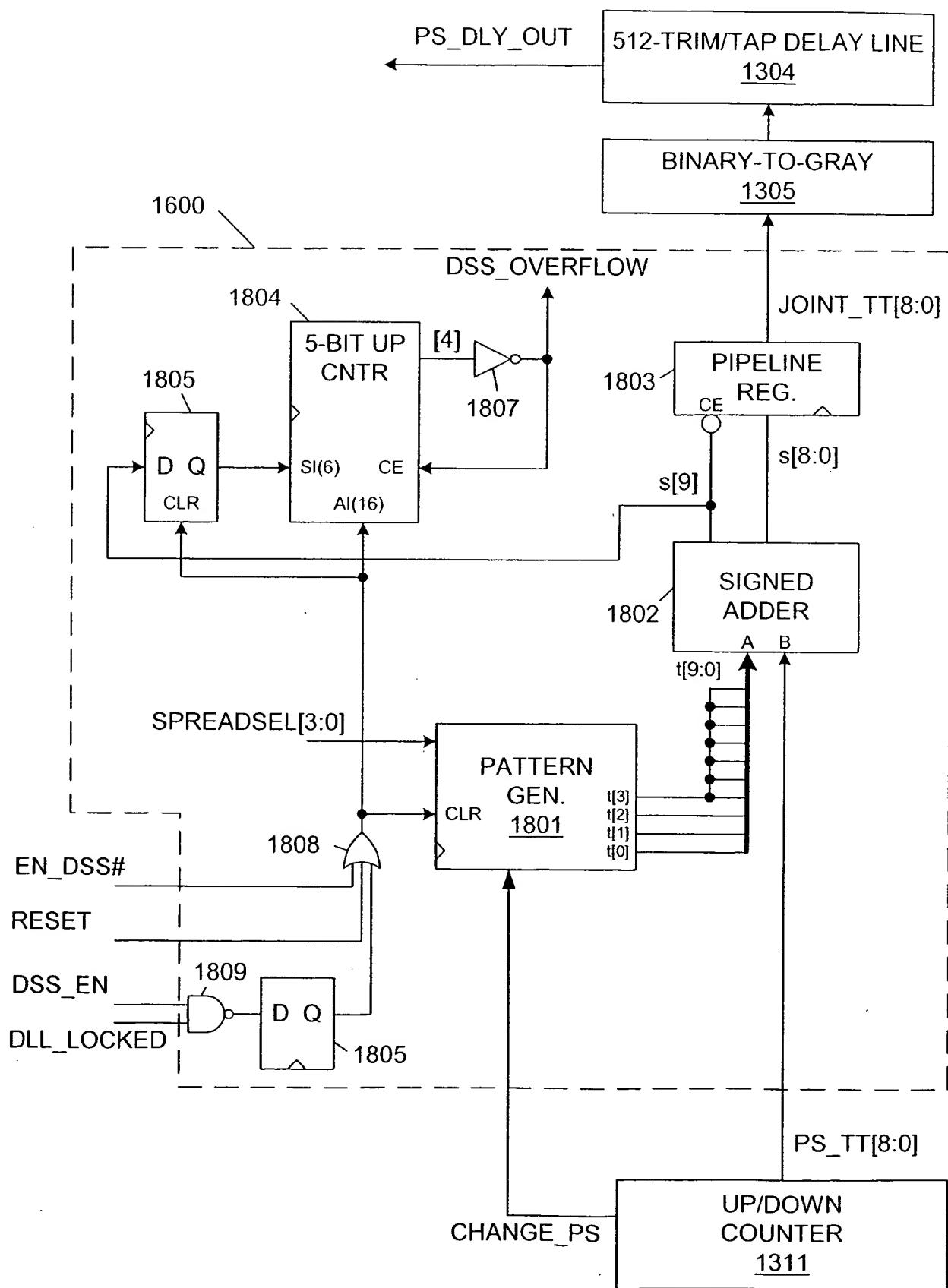


FIG. 18

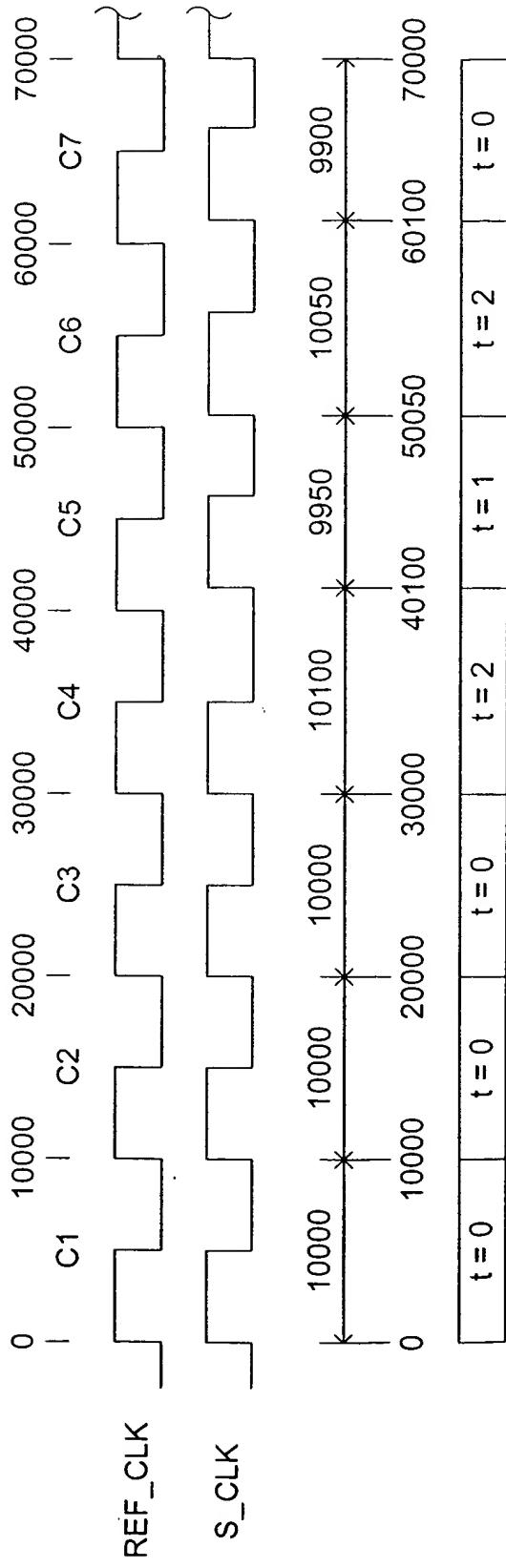


FIG. 19A

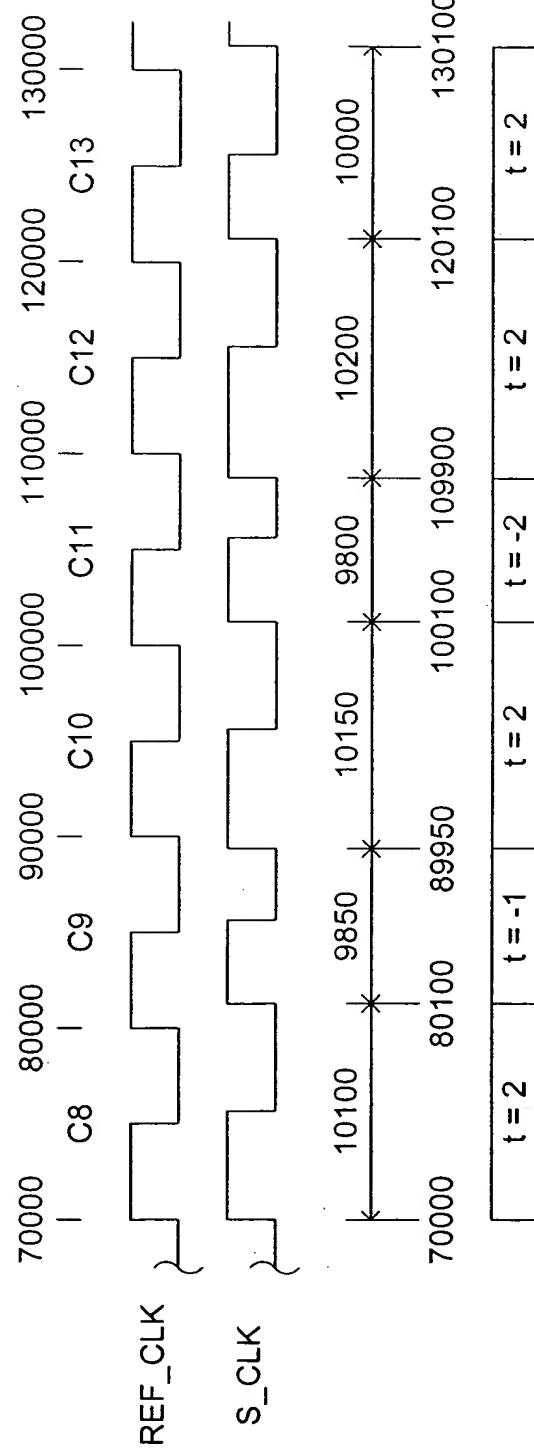


FIG. 19B

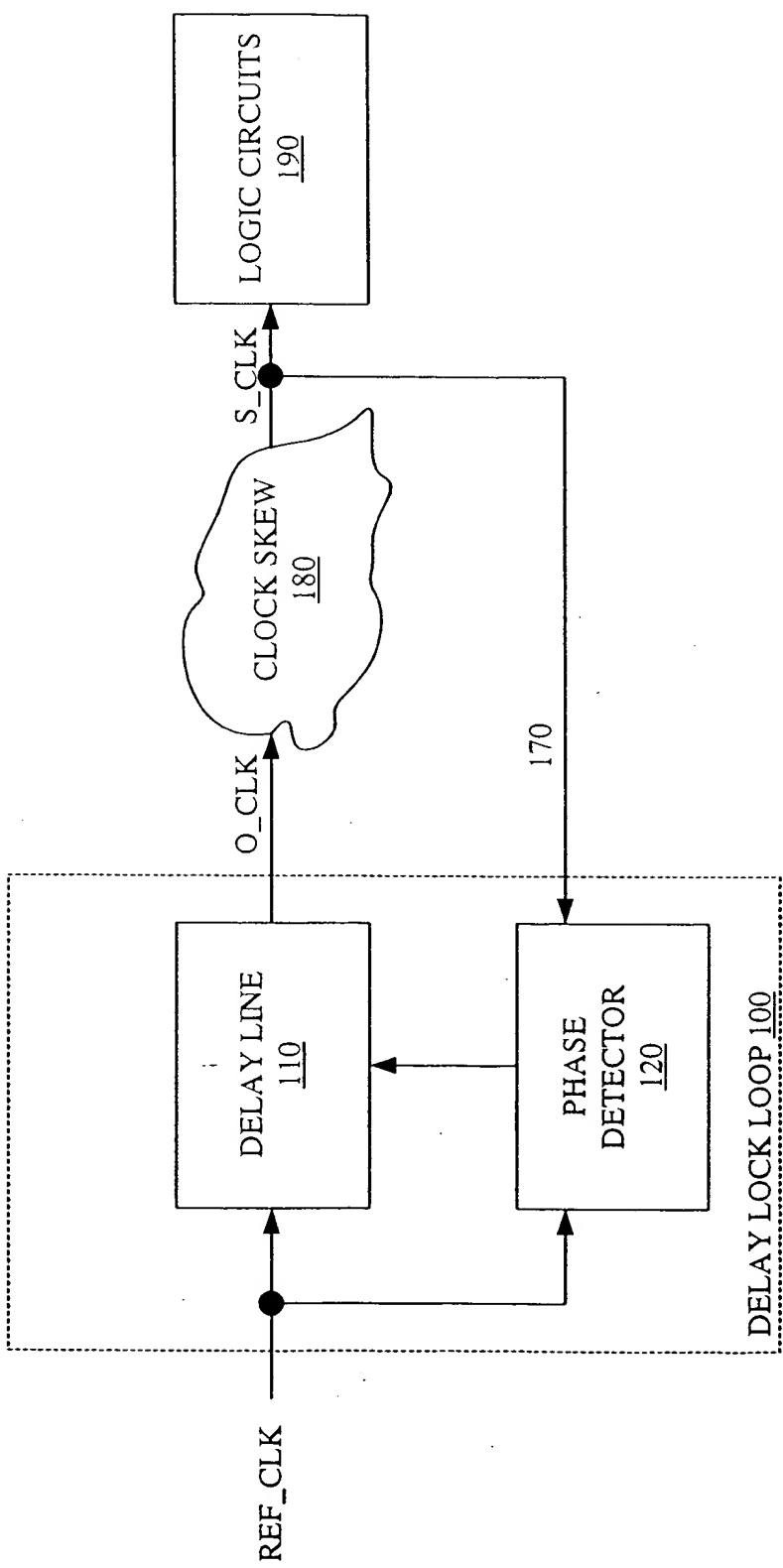


FIGURE 1 (Prior Art)

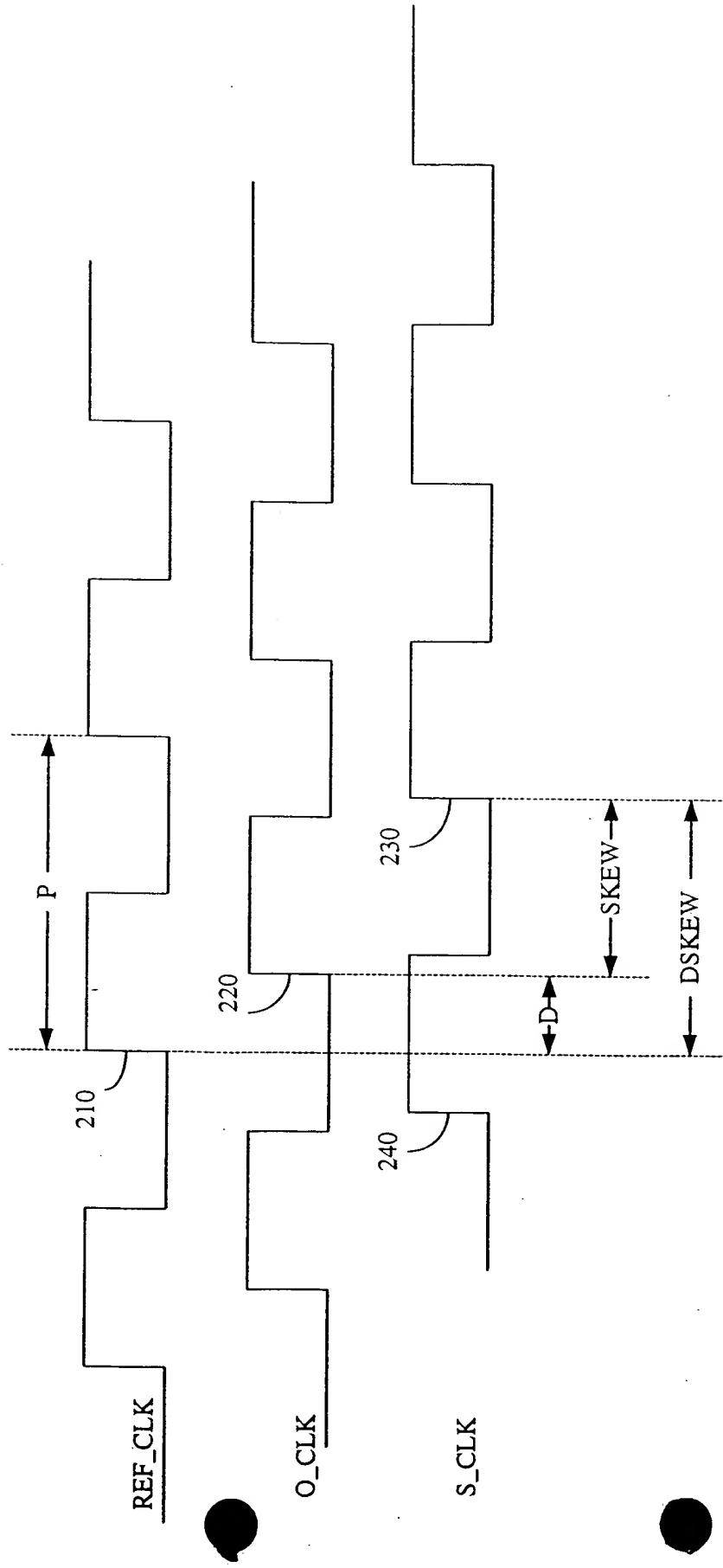


FIGURE 2A